U.S.S.N. 10/767,657

Claim Amendments

Please amend claims 1, 4, 6-12, 13-20, 22-26, and 28-31 as follows:

Please cancel claims 5, 21, and 27 as follows:

Please add new claims 32-34 as follows:

Claims as Amended

What is claimed is:

1. (currently amended) A method of forming a stress relaxed shallow trench isolation (STI) structure to improve charge mobility of a MSOFET device comprising the steps of:

providing a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming ~~one or more~~ a plurality of liner layers comprising

an uppermost plurality of nitride liners selected from the group consisting of silicon nitride (SiN) and silicon oxynitride (SiON) to line the trench;

then forming ~~one or more~~ a plurality of trench filling ~~material~~ oxide layers ~~with stress released material~~, said plurality selected from the group consisting of spin-on glass (SOG) and undoped silicate glass (USG);

wherein at least one stress relaxing thermal annealing step is carried during and following formation of said plurality to form a trench filling substantially free of stress; and,

removing excess trench filling ~~material~~ oxide layers above the trench level.

2\. (original) The method of claim 1, further comprising forming at least one patterned hardmask layer selected from the group consisting of silicon nitride and silicon oxynitride over said substrate.

3. (original) The method of claim 1, wherein the semiconductor substrate comprises material selected from the group consisting of silicon, silicon germanium, and gallium arsenide.

4. (currently amended) The method of claim 1, wherein the ~~one or more~~ plurality of liner layers comprises a lowermost silicon oxide liner ~~are~~ formed according to a method selected from the group consisting of thermal oxidation, LPCVD, and ALCVD.

5. cancelled

6. (currently amended) The method of claim 1, ~~further comprising~~ wherein the step of ~~treating the one or more liner layers with nitrogen (N_2) following the step of~~ forming ~~one or more~~ the uppermost plurality of nitride liners ~~layers according to a treatment selected from the group consisting of a plasma treatment, a thermal anneal, and an implant process in an ambient consisting essentially of nitrogen (N_2) and is~~ comprises a process selected from the group consisting of treating and

underlying thermal oxide liner with nitrogen, and depositing according to a CVD process.

7. (currently amended) The method of claim 1, wherein the step of depositing ~~forming~~ ~~one or more~~ ~~trench filling material~~ USG oxide ~~layers~~ comprises a process selected from the group consisting of SACVD, APCVD, and HDP-CVD~~, and spin coating~~.

8. (currently amended) The method of claim 1 [[9]], wherein the process~~ of spin coating comprises forming a~~ spin-on-glass (SOG) comprises~~ing~~ a precursor selected from the group consisting of organic and inorganic mixtures for forming cross-linked silicon oxide containing structures.

9. (currently amended) The method of claim 8 [[10]], wherein the precursor comprises a material selected from the group consisting of siloxanes, silanes, and polysesilquioxanes.

10. (currently amended) The method of claim 7 [[9]], wherein the SACVD, APCVD, and HDP-CVD processes are carried out

comprising chemical reactants selected from the group consisting of TEOS and O_3.

11. (currently amended) The method of claim 7 [[9]], wherein the SACVD, APCVD, and HDP-CVD processes are carried out comprising chemical reactants selected from the group consisting of SiH_4 and O_2.

12. (currently amended) The method of claim 1, ~~further comprising an intermediate~~ wherein the at least one stress relaxing thermal annealing step thermal annealing step is carried out following formation of each trench filling material layer[[s]] to a desired filling level.

13. (currently amended) The method of claim 1, wherein the step of carrying out at least one stress relaxing thermal annealing step is carried out in an ambient selected from the group consisting of O_2 and N_2.

14. (currently amended) The method of claim 1, wherein the step

of ~~etching~~ forming a trench comprises forming a trench comprising sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

15. (currently amended) The method of claim 1, wherein the step of ~~etching~~ forming a trench comprises forming a trench comprising rounded top and/or bottom corners.

16. (currently amended) A shallow trench isolation (STI) structure with reduced stress to improve charge mobility comprising:

a semiconductor substrate;

a trench formed through a thickness of the semiconductor substrate;

~~one or more~~ a plurality of liner ~~material~~ layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride and silicon oxynitride lining the

trench; and,

~~one or~~ more a plurality of trench filling ~~material~~ oxide layers on the uppermost plurality of nitride liners comprising an SOG layer and an uppermost USG layer ~~silicon dioxide~~, said plurality of trench filling oxide layers substantially free of stress in a direction substantially parallel or perpendicular to the semiconductor substrate major surface.

17. (currently amended) The STI structure of claim 16 [[19]], wherein the trench comprises sidewalls having an angle with respect to a plane parallel to the substrate major surface of between about 80 degrees and about 89 degrees.

18. (currently amended) The STI structure of claim 16 [[19]], wherein the trench comprises rounded top and/or bottom corners.

19. (currently amended) The STI structure of claim 16 [[19]], wherein the ~~one or more~~ the plurality of trench filling ~~material~~ oxide layers comprise[[s]] a portion that extends above the

semiconductor substrate surface.

20. (currently amended) The STI structure of claim 19 [22]], wherein the portion comprises an inward edge portion extending higher above the substrate surface compared to an outward edge portion.

21. cancelled

22. (currently amended) The STI structure of claim 16 [[19]], wherein the one~~-or more trench filling material layers~~ SOG comprises a precursor ~~is~~ selected from the group consisting of siloxanes, silicates, and polysesilquioxanes.

23. (currently amended) The STI structure of claim 16 [[24]], wherein the ~~one or more~~ plurality of trench filling ~~material~~ oxide layers comprises a lowermost SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

24. (currently amended) The STI structure of claim 16 [[24]], wherein the ~~one or more~~ plurality of trench filling ~~material~~ oxide layers comprises a lowermost USG layer, an intervening SOG layer selected from the group consisting of organic and inorganic SOG layers, and an uppermost USG layer.

25. (currently amended) The STI structure of claim 16 [[24]], wherein the ~~one or more~~ plurality of trench filling ~~material~~ oxide layers comprises a plurality of USG layers.

26. (currently amended) The STI structure of claim 21 [[24]], wherein the ~~one or more~~ plurality of trench filling ~~material~~ oxide layers comprises a plurality of SOG layers selected from the group consisting of inorganic SOG layers and organic SOG layers.

27. cancelled

28. (currently amended) The STI structure of claim 16 [[19]], wherein the ~~one or more~~ plurality of nitride liners ~~material~~

~~layers~~ is formed of ~~an SiO_2~~ one of an SiN/SiON and SiON/SiN stack

29. (currently amended) The STI structure of claim 16 [[19]], wherein the ~~one or more~~ plurality of nitride liners ~~material layers~~ is formed ~~of a~~ on an SiO_2~~/SiON~~ ~~stack~~ liner layer.

30. (currently amended) The STI structure of claim 16 [[19]], wherein the ~~one or~~ more plurality of liner ~~material~~ layers is formed of a SiO_2/SiN/SiON stack.

31. (currently amended) The STI structure of claim 16 [[19]], wherein the ~~one or more~~ plurality of nitride liners ~~material layers is formed of~~ comprises one of a SiN/SiON and SiON/SiN stack.

32. (new) The method of claim 1, wherein the plurality of nitride liners comprises one of an SiN/SiON and SiON/SiN stack of layers.

33. (new) A method of forming a stress relaxed shallow trench isolation (STI) structure to improve charge mobility of a MSOFET

device comprising the steps of:

a) providing a semiconductor substrate;

b) forming a trench in the semiconductor substrate;

c) forming a plurality of liner layers comprising an uppermost plurality of nitride liners selected from the group consisting of silicon nitride and silicon oxynitride to line the trench;

d) then forming a first silicon oxide layer to partially fill said trench;

e) then annealing said first silicon oxide layer to relax a stress within said first silicon oxide layer;

then repeating steps d) through e) at least once to form subsequent silicon oxide layers to fill said trench with a plurality of stress relaxed oxide layers.

34. (new) The method of claim 33, wherein the plurality of stress relaxed oxide layers is selected from the group consisting of SOG and USG oxide.